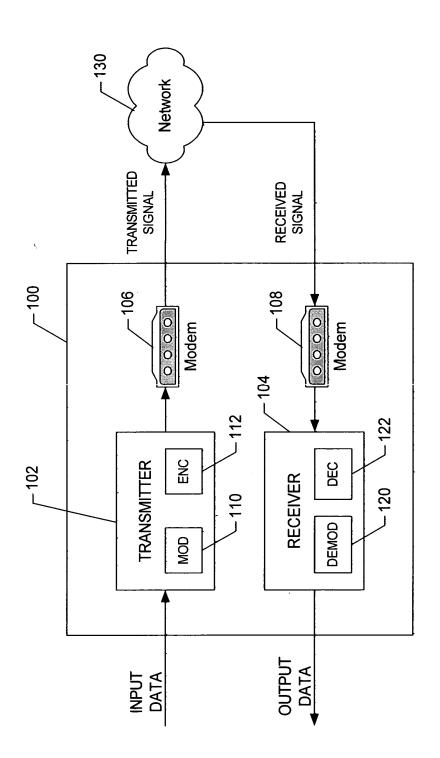Heller Ehrman White & McAuliffe LLP
Title: "HIGH DATA RATE COMMUNICATION SYSTEM
FOR WIRELESS APPLICATIONS"
Inventor(s): A. Kumar
Atty Docket No.: 39908-6214
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FIGURE 1

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Inventor(s): A. Kumar
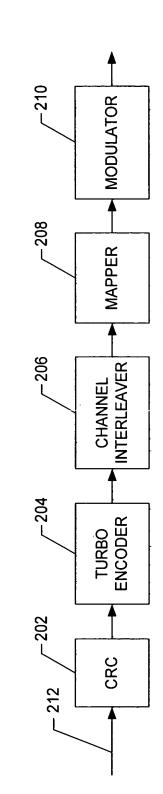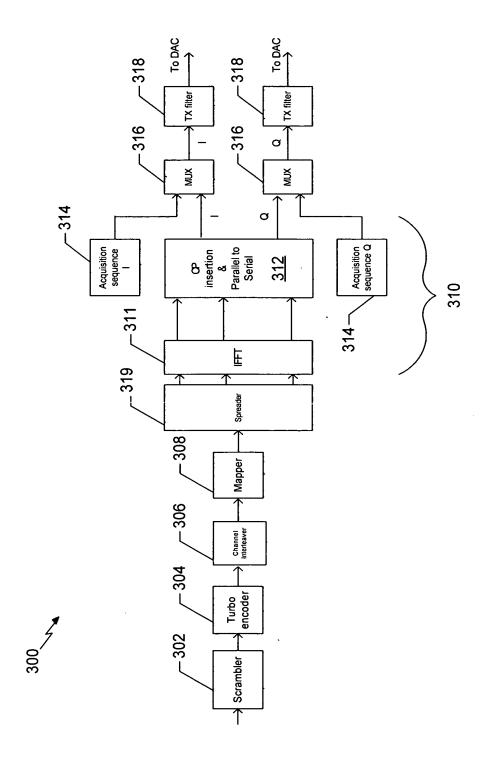Atty Docket No.: 39908-6214
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FIGURE 2

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FIGURE 3

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FIGURE 4

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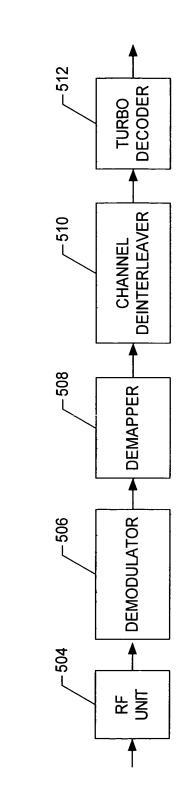504 RF UNIT

506 DEMODULATOR

508 DEMAPPER

510 CHANNEL DEINTERLEAVER

512 TURBO DECODER

FIGURE 5

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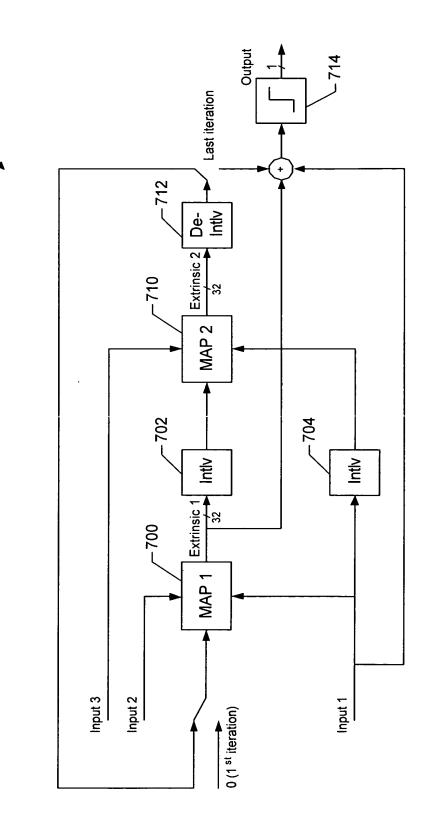FIGURE 6

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FIGURE 7

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FIGURE 8

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FOR WIRELESS APPLICATIONS"
Inventor(s): A. Kumar
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```
                    ┌─────────────┐
                   (    START      )
                    └─────────────┘
                           │
                           ▼
    ┌───────────────────────────────────────────┐
    │ Perform backward recursion on the trellis by computing │── 900
    │        backward state metrics (beta)        │
    └───────────────────────────────────────────┘
                           │
                           ▼
    ┌───────────────────────────────────────────┐
    │     Store the backward state metrics to a storage     │── 902
    │                  mechanism                  │
    └───────────────────────────────────────────┘
                           │
                           ▼
    ┌───────────────────────────────────────────┐
    │  Perform forward recursion on the trellis by computing │── 904
    │        forward state metrics (alpha)        │
    └───────────────────────────────────────────┘
                           │
                           ▼
    ┌───────────────────────────────────────────┐
    │          Calculate extrinsic information          │── 906
    └───────────────────────────────────────────┘
                           │
                           ▼
                    ┌─────────────┐
                   (     END       )
                    └─────────────┘
```

FIGURE 9

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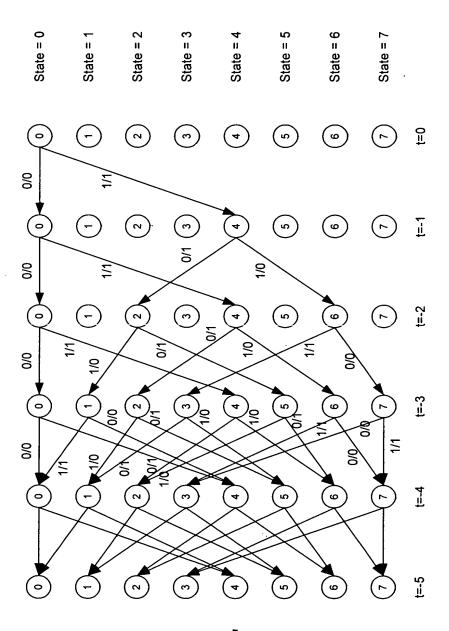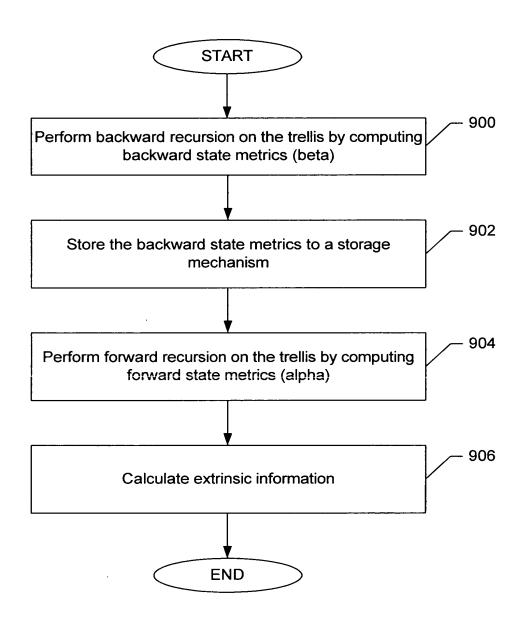Inventor(s): A. Kumar
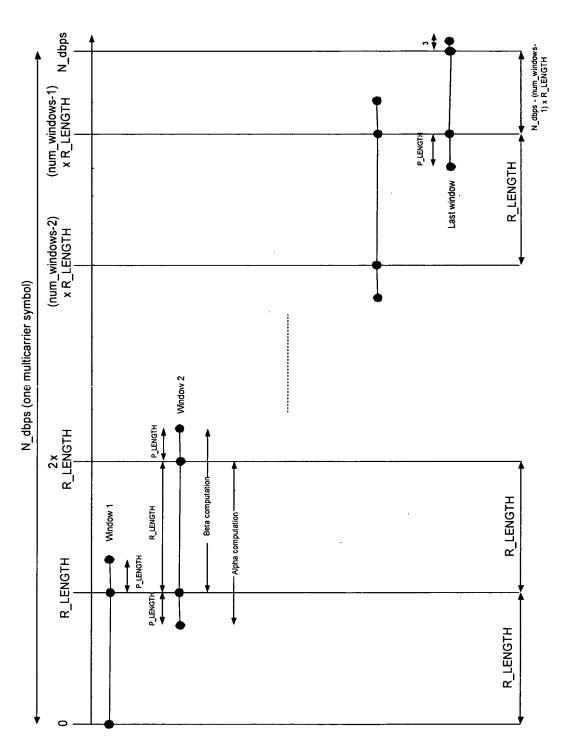Atty Docket No.: 39908-6214
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FIGURE 10

Beta	x+3	x+2	x+1	x	x-1	x-2	x-3	x-4	x-5	x-6	x-7	x-8	x-9	x-10	x-11	x-12
Stored Beta				x				x-4				x-8				x-12
Beta recovered during extrinsic information computation																
Cycle (n+0)	Compute x+1 and x+2															
Cycle (n+1)	Compute x+3															
Cycle (n+2)	The decoder uses x+3 and x+2. Compute x-3 and x-2															
Cycle (n+3)	The decoder uses x+1 and x. Compute x-1															
Cycle (n+4)	The decoder uses x-1 and x-2. Compute x-7 and x-6															
Cycle (n+5)	The decoder uses x-3 and x-4. Compute x-5															
Cycle (n+6)	The decoder uses x-5 and x-6. Compute x-11 and x-10															
Cycle (n+7)	The decoder uses x-7 and x-8. Compute x-9															
Cycle (n+8)	The decoder uses x-9 and x-10. Compute x-15 and x-14															

FIGURE 11

	x+3	x+2	x+1	x	x-1	x-2	x-3	x-4	x-5	x-6	x-7	x-8	x-9	x-10	x-11	x-12
Beta	x+3	x+2	x+1	x	x-1	x-2	x-3	x-4	x-5	x-6	x-7	x-8	x-9	x-10	x-11	x-12
Stored Beta		x+2		x		x-2		x-4		x-6		x-8		x-10		x-12
Beta recovered during extrinsic information computation																
Cycle (n+0)			Compute x+1													
Cycle (n+1)			The decoder uses x+1 and x.		Compute x-1											
Cycle (n+2)			The decoder uses x-1 and x-2.				Compute x-3									
Cycle (n+3)			The decoder uses x-3 and x-4.						Compute x-5							
Cycle (n+4)			The decoder uses x-4 and x-5.						Compute x-5							
Cycle (n+5)			The decoder uses x-5 and x-6.								Compute x-7					
Cycle (n+6)			The decoder uses x-7 and x-8.										Compute x-9			
Cycle (n+7)			The decoder uses x-9 and x-10.												Compute x-11	
Cycle (n+8)			The decoder uses x-11 and x-12.													Compute x-13
▫ ▫ ▫																

FIGURE 12

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FIGURE 13

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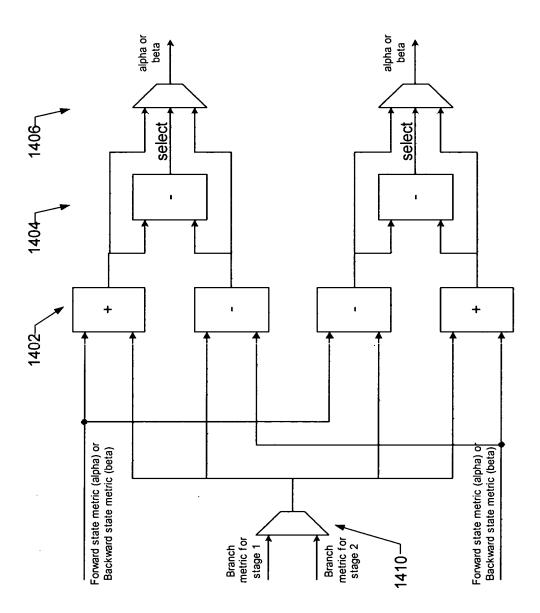Inventor(s): A. Kumar
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FIGURE 14